Silicon Gate CMOS **5204**

TIME/SECONDS/DATE LIQUID CRYSTAL DISPLAY DECODER-DRIVER

- **Displays Hours and Minutes or Seconds or Date**
- **Pin Compatible with Intel 5201 and 5202**
- **Advanced Silicon Gate Ion Implanted CMOS Technology**
- **Anti-Bounce Circuitry on Switch Inputs**
- **Drives 3½ Digit Field Effect Displays**
- **Inputs Protected Against Static Discharge**

The 5204 is a low power 3-½ digit liquid crystal display decoder driver intended for use in 12 hour timekeeping applications such as wristwatches and battery-operated clocks.

The 5204 accepts a 64 Hz input signal from which it counts and decodes Seconds, Minutes, Hours, and Date. The decoded signals are used for driving the three 7-segment and one 2-segment display digits. A symmetrical 32 Hz signal is provided to drive the common back plate of the display. Segments to be energized are driven with a symmetrical 32 Hz signal that is out-of-phase with the common signal while unenergized segments are driven with a 32 Hz signal in phase with the common signal.

The 5204 will normally display Hours and Minutes. Depression of the D/C command switch will cause Seconds to be displayed in the Minutes position and the Hours will be blanked. A second depression of the D/C command switch will cause the Date to be displayed in the Minutes position and the Hours to be blanked. A third depression of the D/C command switch will cause a return to normal mode displaying Hours and Minutes. The colon is flashed at a 1 Hz rate in all three display modes.

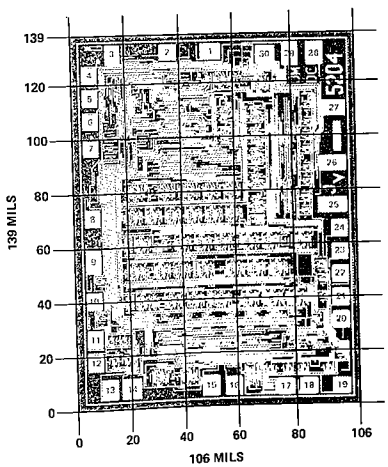
A separate switch is used for timesetting. Thus only two switches are required for operation of the watch. (See page 8-9 for description of operation.)

The 5204 is designed to operate in conjunction with the 5801 oscillator-divider circuit. For information on the 5801 see the 5801 data sheet.

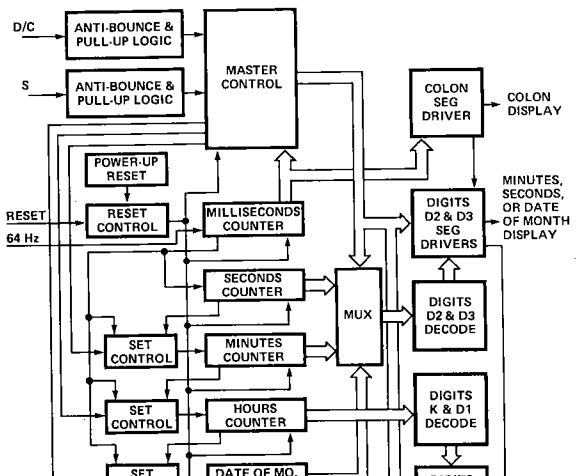
This device is fabricated with complementary MOS silicon gate technology. This extremely low power technology is ideally suited for the manufacture of devices designed to operate from small batteries for long periods of time.

CHIP TOPOGRAPHY

(Numbers refer to package pin number.)



BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... −20°C to +70°C
Storage Temperature ..... −40°C to +125°C
Supply Voltage V_{DD} with respect to GND ..... −0.3V to +18.0V
Voltage on all Inputs or Outputs with respect to GND ..... −0.3V to V_{DD} +0.3V
Power Dissipation 100mW

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 25°C$; $6V \leq V_{DD} \leq 10V$; $f_{in} = 64$ Hz, Unless Otherwise Specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
I_{DD}	Total Average Internal Current		500	nA	$V_{DD} = 10V$; $t_{pwc} = 25\mu s$; $t_f = 0.5\mu s$; $t_r = 75\mu s$; Outputs Open
I_{ILC}	64 Hz Input Low Current (Clock)	2.0	-15	μA	$V_{DD} = 10V$; $V_{IN} = 1.2V$
I_{ILS}	Switch Input Low Current (D/C, S)	-1.0	-50	μA	$V_{DD} = 10V$; $V_{IN} = 1.2V$ 64 Hz Input Voltage = 0.0V Note 1
V_{IL}	Input Low Voltage	-0.3	1.2	V	
V_{OLC}	Output Low Voltage Common		25	mV	$V_{DD} = 10V$; $I_{OLC} = 1.0\mu A$
V_{OHC}	Output High Voltage Common	V_{DD}-.025		V	$V_{DD} = 10V$; $I_{OHC} = -1.0\mu A$
V_{OLS}	Output Low Voltage Segment		25	mV	$V_{DD} = 10V$; $I_{OLS} = 0.1\mu A$
V_{OHS}	Output High Voltage Segment	V_{DD}-.025		V	$V_{DD} = 10V$; $I_{OHS} = -0.1\mu A$
I_{ILR}	Reset Input Low Current	-1.0	-200	μA	$V_{DD} = 10V$

A.C. Characteristics

$T_A = 25°C$; $6V \leq V_{DD} \leq 10V$; $f_{in} = 64$ Hz, Unless Otherwise Specified

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{pwc}	Input Pulse Width (Clock)	10	25	μs	$V_{IL} = 1.2V$
t_f	Input Pulse Fall Time		0.5	μs	$V_{DD} = 10V$; $V_{IL} = 1.2V$; $V_{IH} = 9V$
t_r	Input Pulse Rise Time		75	μs	$V_{DD} = 10V$; $V_{IL} = 1.2V$; $V_{IH} = 9V$
t_{sd}	Switch Delay	32	80	ms	Note 2

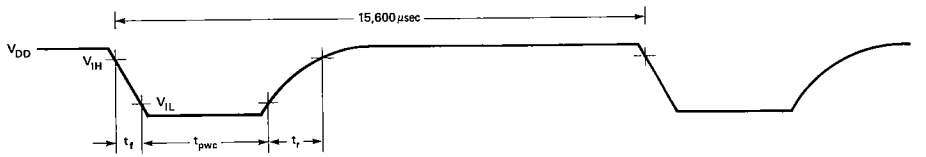
Capacitance ($T_A = 25°C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		2.8	5	pF	Capacitances are measured in 30 lead flatpack with all pins except the test pin at ground, f = 1MHz.
C_{OUTC}	Output Capacitance Common		8.5	15	pF	
C_{OUTS}	Output Capacitance Segments		2.0	5	pF	

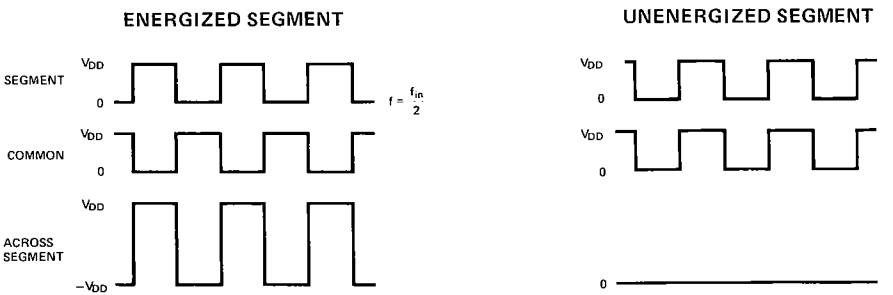
NOTES: 1. All switch inputs include dynamic pull-up circuitry which is clocked in synchronization with the 64 Hz input. The average current drawn by these inputs in the low state will be proportional to the duty cycle of the 64 Hz input. The value specified is for the case where the 64 Hz input is held low. (100% duty cycle).

2. The D/C and S switch inputs include anti-bounce circuitry. This circuitry requires that a switch input be stable for 2 consecutive 32 Hz clock periods in order to be recognized as a valid input. Switch delay is the time during which the antibounce circuitry is determining a valid, stable input.

Input Waveform

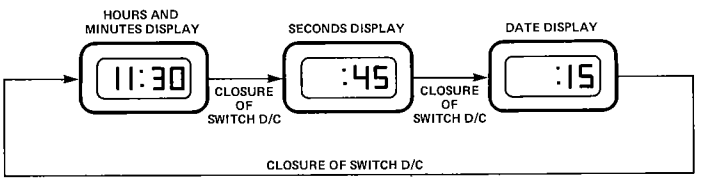


Output Waveforms



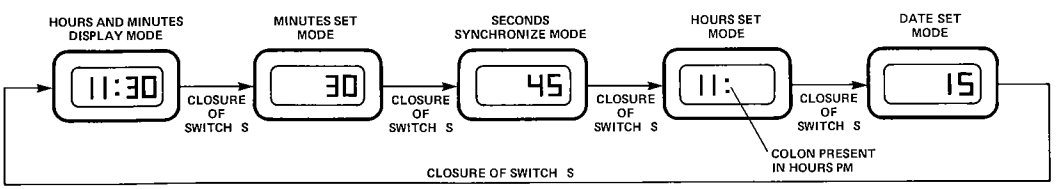
Time Display

Switch input D/C controls the time display modes. Each closure of switch D/C (D/C input = low) causes a change in the display mode in the sequence Hours and Minutes → Seconds → Date → Hours and Minutes. The following diagram illustrates this:



Time Setting

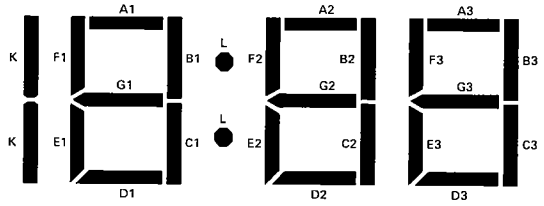
Switch input S controls the time setting modes. This switch input is active only when the circuit is in the Hours and Minutes display mode. Each closure of switch S (S input = low) causes a change in the time set modes in the sequence Hours and Minutes → Minutes → Seconds → Hours → Date → Hours and Minutes. *Closure of switch D/C when in the Minutes, Hours, or Date time set modes will cause that mode to be advanced at a 1 Hz rate. Closure of switch D/C in the Seconds synchronize mode will cause the Minutes to be advanced by one and the Seconds to be reset to zero and held until the D/C input is returned high.* The colon is displayed only in the Hours PM state in the time set mode. The following diagram illustrates this:



Reset

The reset input may be used to initialize all time counters to the zero state. All time counters are automatically reset to zero when voltage is initially applied to the circuit. The zero state is 12:00 AM, 00 Seconds, 0 Date.

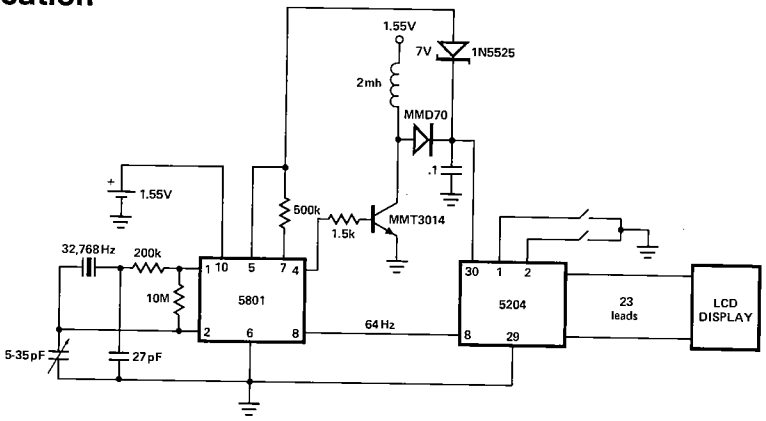
Display Segment Format



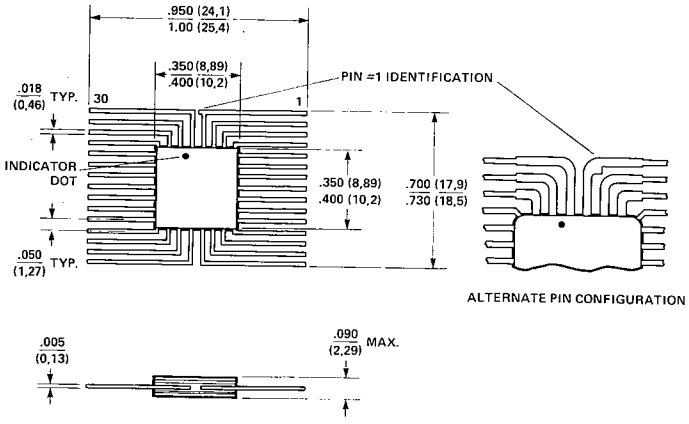
DIGITS D1, D2 AND D3 TRUTH TABLE

NUMBER	SEGMENTS						
	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Typical Application



Packaging Information



PIN ASSIGNMENT

Pin No.	Function	Pin No.	Function
1	D/C	16	N/C
2	S	17	B3
3	Common	18	A3
4	K	19	F3
5	E1	20	G3
6	D1	21	B2
7	C1	22	A2 + D2
8	64Hz In	23	F2
9	L (Colon)	24	G2
10	E2	25	B1
11	C2	26	A1
12	E3	27	F1
13	D3	28	G1
14	C3	29	Ground
15	Reset	30	V_{DD}